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On-site diagnostic of insulating down conductors

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***Abstract*— Insulating Lightning Protection Systems (LPS) are widely used in different applications like mobile radio, industrial equipment or process industries. For the erection of such insulating LPS very often GFRP components as well as insulating down conductors are used. The use of an insulating down conductor becomes more and more relevant in lightning protection of buildings where architectural restrictions apply.**

It seems to be logic that the functionality of the components used in those insulating LPS has to be checked periodically. In insulating LPS where GFRP components are used a simple visual inspection is checking the mechanical condition. This simple visual inspection may not be sufficient in insulating LPS with insulating down conductors where a potential insulation damage may be very small and possibly inside the down conductor.

Insulating down conductors based on coaxial structure with a low conductive coating are different from aerial or energy cables. A good conducting cover acts as a coaxial back conductor and allows the propagation of travelling waves within the cables. These travelling waves, however, cannot exist on structures with low conducting cover. The analysis of these travelling waves are the basis for the application of fault location methods used at HF and power cables. For that reason these methods cannot be applied.

Obviously all established fault detection procedures which use the propagation of signals in soil are not applicable.

The paper presents different electric methods of on-site dielectric testing of insulation failures in insulating down conductors.

According to today's state of technology these procedures require the provocation of a minimum insulation failure on-site.

Numerous investigations on damaged insulating down conductors have shown that the existence of an insulation fault can be proved by impulse testing with comparatively low voltage and energy.

Different methods of fault detection are discussed by means of lab tests.

Finally the paper presents a simplified integral electrical test method to check the insulation capability of the insulating down conductor on-site. The test method is based on the evaluation of the time constant of the test circuit in presence of an insulation fault. The results of first on-site tests using this method are discussed.

Keywords-insulating down conductor; on-site testing; SPICE Simulation; electromagnetic modelling;

I. INTRODUCTION

Insulating down conductors (IDCs) which today are increasingly used in "insulating lightning protection systems" resemble in their structure cables which are used in the energy and high-frequency (HF) applications. In these applications fault detection and location procedures have been state of the technology for a long time [1].

It seems reasonable to check these procedures also for their applicability to fault diagnostics on IDCs and if necessary to derive new methods from it. The largest group of these methods bases on the coupling of an electromagnetic wave into the cables and the evaluation of signals refracted and/or reflected of the fault location. To assess the applicability and limits of these methods, it is necessary to examine the electromagnetic wave propagation on IDCs more precisely. For this purpose an electromagnetic model of IDCs is evaluated using a lattice network approach. The transient behavior of the fault location itself is modelled by means of the constant area criterion [2].

II. ELECTROMAGNETIC MODELLING OF IDCS

IDCs bear resemblance to energy or HF cables (coaxial cable) within this coaxial structure. A lattice network approach of such a coaxial structure is shown in Fig. 1.

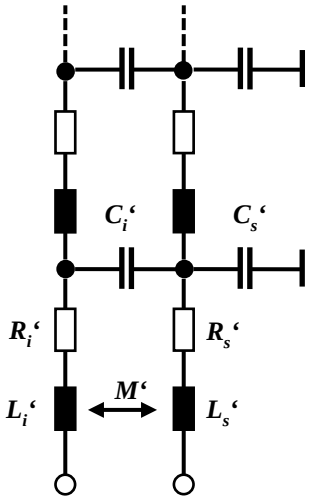

Figure 1. Lattice network of a coaxial structure

The lattice network parameters of a representative IDC with a diameter d ≈ 2 cm is given in TABLE I.

The parameters in TABLE I demonstrate the relationship of IDCs with coaxial cables. These parameters are identical for coaxial cables and IDCs with equivalent dimensions apart from one exception – the resistance load per unit length of the sheath R_s'. The fundamentals of this construction are described in [3].

TABLE I. LATTICE NETWORK OF A REPRESENTATIVE IDC

	Network Parameters of IDC ($d \approx 2$ cm)		
Ohmic	$R_i' = < 1$ mΩ/m	$\boldsymbol{R_s' \approx 2}$ **kΩ/m**	
Capacitive	$C_i' \approx 100$ pF/m	$C_s' \approx 12$ pF/m	
Inductive	$L_i' \approx 1{,}15$ µH/m	$L_s' \approx 0{,}9$ µH/m	$M' \approx 0{,}9$ µH/m

A. *Different behavior of IDC and coaxial cable*

Typical IDCs show a R_s' in the range of some kΩ/m. This serious resistance load per unit length of the sheath avoids significant current flow on the sheath of the IDC and also avoids dangerous current flows into the building where it is mounted.

However a good conducting sheath is used at coaxial cables. This leads to a generally different behavior with regard to the propagation of electromagnetic waves resulting in different lattice networks for coaxial cables and IDCs (see Fig. 2).

The path of current flow is red marked in Fig. 2. This results in an effective inductance per unit length $L'_{coax} = L_i' + L_s' - 2M' = L_i' - L_s' \approx 0{,}25$ µH/m. The link with effective capacitance per unit length $C_i' \approx 100$ pF/m results in a wave impedance of $Z_W = 50\ \Omega$ that is typical for coaxial cables. I. e. the complete field energy propagates in the dielectric of the coaxial cable. There is practically no electromagnetic field in the surroundings.

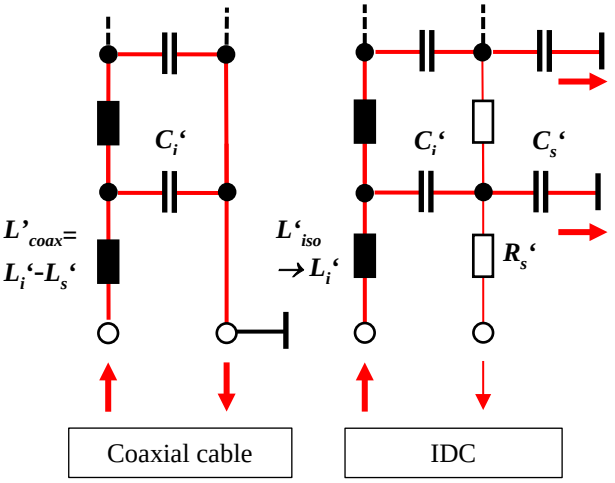

Figure 2. Coaxial cable vs. IDC - Comparison of lattice networks

The field propagation at an IDC behaves completely different. With rising frequency (shorter rise time) the field energy leaves the coaxial structure and spreads out to the outside space (see also current paths in Fig. 2). The electromagnetic behavior of an IDC is similar to monopole antenna. If the current on the sheath can be neglected the resulting effective inductance per unit length is $L'_{iso} \rightarrow L_i' \approx 1{,}15$ µH/m. The effective capacitance results from the series connection of C_i' und C_s' ($C'_{res} = 10{,}7$ pF/m). In this case the wave impedance is about $Z_{iso} \approx 330\ \Omega$ which meets approximately the value for a structure in the free space.

B. *Fault Detection Possibilities*

IDCs may be damaged by mechanical or dielectric overloads or by mistakes done during installation. Whereas mechanical damage, e.g. too small bending radii, scratches or cuts during installation may be discovered by inspection during or after the installation itself, a loss of insulation capability is much harder to detect. Dielectric overloads may occur if the IDC is e.g. exposed to lightning currents exceeding the declared parameters which is most likely at subsequent strokes due to the higher induced voltages compared with first strokes.

A picture of a typical dielectric defect which could be caused by dielectric overload is shown in Fig. 3. The size of such a defect constitutes some millimeters.

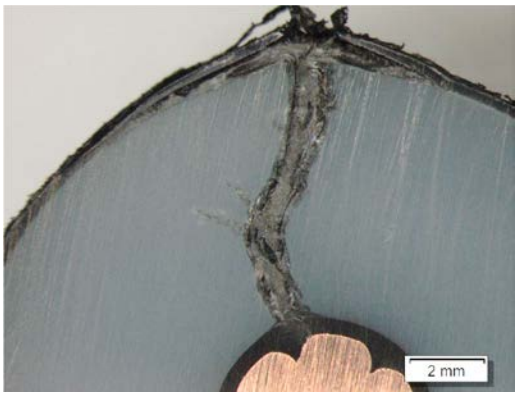

Figure 3. Dielectric defect in an IDC

In the case of the coaxial cable this defect represents a significant electromagnetic field disturbance which can be detected and located by means of the known methods.

In the case of IDCs the remaining volume density of electromagnetic energy in the dielectric is comparatively low. Therefore there are no refracted and/or reflected signals from the dielectric defect in the IDC which could be used for fault detection or location. Due to the specific electromagnetic features of an IDC explained above it is impossible to detect dielectric defects in IDCs with electromagnetic fault diagnostic methods commonly used at coaxial cables.

In the case of a dielectric defect the original dielectric strength is diminished by magnitude order. This allows a new approach that stimulates the defect in such a way that evaluable signals are sent out from its location. A practical way is to increase the electric field strength in the IDC until a small discharge appears at the fault position. The nonlinear effects caused by the discharge are evaluated and can be used for the fault detection. One of the most important topics is to find a suitable test impulse with high detection efficiency and minimal energy. Therefore it is not desirable to apply the waveforms of first or subsequent strokes for on-site testing.

III. FAULT DETECTION AT IDCS

The size of typical IDC installations is in the range of some 10 meters. This size can be considered as long compared to the smallest wavelength given by the test impulse. Therefore a model based on lumped elements is applicable.

A. *Test circuit*

A test impulse U_{gen} with sufficient energy and voltage in order to create a small discharge at the fault position is fed at the ground connection of the IDC. In case of a more complex IDC system with more than one earth connection, the other earth connections have to be disconnected and insulated in a safe way. The model based on lumped elements is shown in Fig. 4.

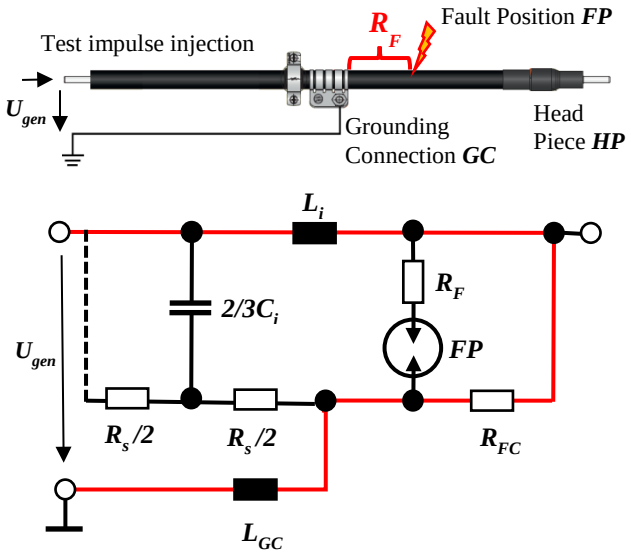

Figure 4. Test impulse injection for fault detection in IDC - Model with lumped elements

Modelling of the C_i, R_s – lattice structure was adopted from the modelling of parasitic capacitors at high voltage dividers [5]. Many IDCs use a grounding connection (L_{GC}) for potential grading and field control which is done in the section between the head piece *HP* and the grounding connection *GC*. This section is represented by R_{FC}. The main test impulse current path is indicated in red. Defects due to abnormal dielectric stress occur at locations with high electric fields. Hence a fault in the vicinity of the grounding connection is most likely (indicated as *FP* in Fig. 4). The existence of such a fault due to an insulation defect is included in the equivalent circuit by an additional resistor R_F which is activated by the discharge at *FP*.

A compromise between the choice of the energy and the voltage level of the test impulse has to be found. On one side the levels must be sufficient that the discharge appears for sure, on the other side unnecessary high levels must be avoided for safety and EMC reasons. In order to find the right compromise it is necessary to analyze and model the characteristics of the dielectric defect *FP* in more detail.

B. *Modelling a defect in an IDC*

In order to analyze and model dielectric defects in IDCs lab experiments with several small primed test samples (see Fig. 5) were performed. The test samples were gained from IDCs that did not pass the high voltage impulse test for insulating down conductors as it is intended in the future IEC 62561-8. This test procedure is described in more detail in [4].

The experiments showed that small discharges can be produced using impulse voltages with 9-17 kV peak with a time to breakdown $T_B < 2\mu s$. There was a significant statistical spread in the results. Therefore it is suggested to use impulse voltages with a voltage level that remains at least 2 µs above 20 kV. For all of our test samples a test impulse like this guarantees the discharge at the defect location. This discharge is the one and only nonlinear effect at this voltage level which can be used for istinct fault detection.

Figure 5. Primed test sample with insulation defect

A good preexisting model for this discharge is the constant area criterion (CAC) evaluated by D. Kind [2].

$$\int (u(t) - U_0)\,dt = A \qquad (1)$$

$$\text{with} \quad U_0 > 8\ \text{kV} \ \text{and} \ \ A > 4\ \text{mVs}$$

This model can be transformed easily in an equivalent electric circuit for the use with analog circuit simulators. A simple realization with U_0 = 9,5 kV and A_{ref} = 5 mVs created in LTSPICE [6] is shown in Fig. 6.

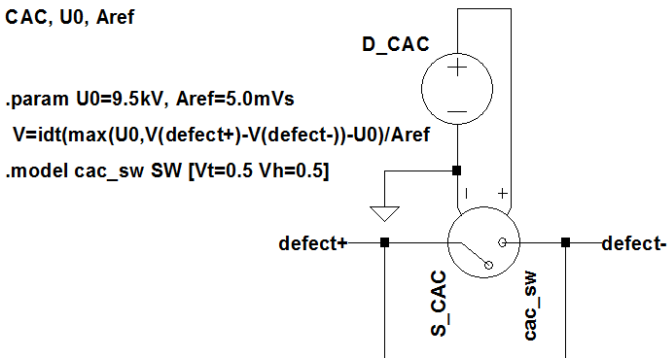

Figure 6. SPICE Model of insulation defect

The evaluation of the CAC according to (1) requires the solution of the integral with the start condition when $u(t)$ exceeds U_0. The discharge starts when the integral reaches A_{ref}. In the SPICE simulation this is realized by a controlled voltage source evaluating expression (2) triggering a voltage controlled switch (with threshold $V_t + V_h$ = 1 V).

$$\int \left(\max(u_{defect+}(t) - u_{defect-}(t), U_0) - U_0\right) dt / A_{ref} \geq 1 \qquad (2)$$

C. Direct Detection Methods / Lab Test

In this section the possibilities of fault detection are discussed. As a first step a test setup was arranged in the high voltage lab. Short samples of IDCs with 2 m length and implemented insulation defaults were used. The resistance load per unit length of the sheath was $R_s' = 2{,}2$ kΩ/m. The fault position FP was 10 cm apart the grounding connection *GC*. A picture of this test setup is given in Fig. 7.

Figure 7. Lab test setup for defect detection

The equivalent circuit of this lab test setup is shown in Fig. 8. This consists of a simple impulse generator circuit and a test sample of an IDC as described above. Injected voltage u_{gen} and current i_{gen} were measured and digitized. Furthermore the electromagnetic field in the vicinity of *FP* was measured by means of a small dipole antenna.

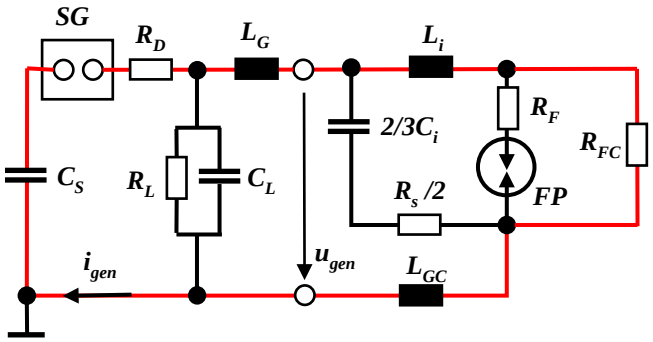

Figure 8. Equivalent circuit of lab test setup for defect detection

The results of these measurements are shown in Fig. 9. The appearance of the small discharge at the fault location at $t = 1{,}7$ µs can be detected easily in the voltage, current and field trace. So any of these 3 measures is appropriate to detect the defect.

In addition the test setup was simulated in SPICE using the equivalent circuit shown in Fig. 8 and the model of the insulation defect according to Fig. 6. The result is plotted as red graph in the voltage and current trace in Fig. 9. There is a good correlation between experiment and simulation. So this simulation model is also a good tool for the preparation of on-site tests.

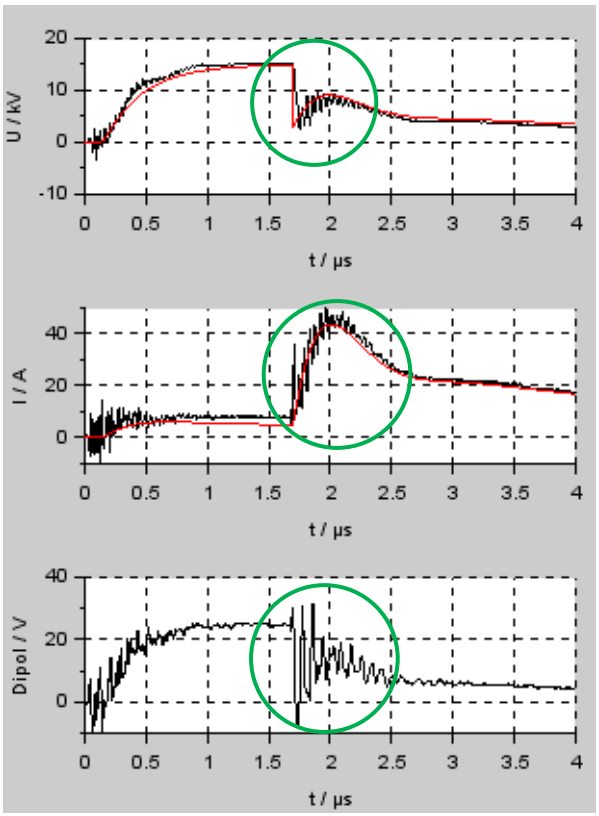

Figure 9. Lab measurements at 2 m samples
Fault detection by use of
- voltage measurement u_{gen} at impulse generator (upper trace)
- current measurement i_{gen} at impulse generator (middle trace)
- electromagnetic field measurements (lower trace)

Evaluation of transient processes is shown in Fig. 9 and they are easy to perform in the lab. At on-site testing, however, a more robust and also less sophisticated approach is desirable. For that reason the integral test method was developed that evaluates a long period of record.

D. Integral Detection Method

One of the measurands which is easy to access even at on-site testing is the voltage U_{CS} at the surge capacitor in the impulse generator. The idea behind the integral method is the long term evaluation of $u_{CS}(t)$. Long time recording at lower bandwidth of just one single measurand is also beneficial for the necessary test equipment which makes it simpler and affordable.

At the testing of IDCs transient processes decay within some µs. The observation period within the integral detection method is at least some tens of µs. The negligence of all transient processes simplifies the equivalent circuit described in Fig. 8. Using a generator circuit of typical design with $R_D << R_L$ and $C_L << C_S$ results in a simple resistive discharge circuit of C_S.

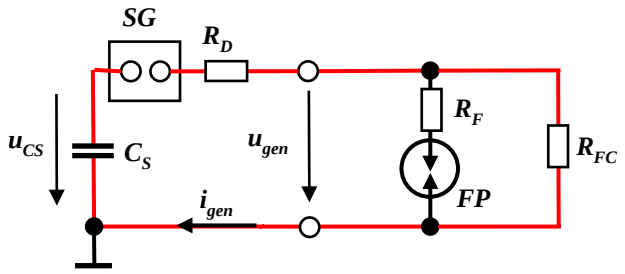

Figure 10. Simplified circuit for integral defect detection

The long term voltage at C_S during the discharge process is given by the well-known formula (3).

$$u_{CS}(t) = U_{CS0} \cdot e^{-t/\tau} \tag{3}$$

with U_{CS0} = initial charging voltage of C_S and $\tau = C_S R_{tot}$

A discharge at *FP* leads to a different R_{tot} and τ indicating defect in the IDC – this is given in (4).

$$R_{tot} = R_D + R_{FC} \quad \text{(no defect at } FP\text{)} \tag{4}$$

$$R_{tot} = R_D + \frac{R_F \cdot R_{FC}}{R_F + R_{FC}} \quad \text{(with defect at } FP\text{)}$$

The integration of (3) over a significant long period and normalization on the initial charging voltage U_{CS0} of C_S reveals τ - as evaluated in (5).

$$\frac{\int_0^{t\to\infty} u_{CS}(t)dt}{U_{CS0}} = \tau \tag{5}$$

The integral defect detection is performed by 2 sequential tests with different U_{CS0} levels. The first test is done with a low U_{CS0} level (< 1kV). At this level no discharge occurs at FP even if a dielectric defect exists. The evaluation of (5) on the first test offers a reference τ_1. The second test is done with a high U_{CS0} level (> 20kV). A new evaluation of (5) yields a second τ_2. If there is no dielectric defect the IDC behavior is linear within this voltage range and $\tau_1 = \tau_2$.

If a dielectric defect exists at *FP* a small discharge is evoked at the second test with a high U_{CS0} level. This nonlinear effect causes a reduced R_{tot} and $\tau_1 > \tau_2$. The decrease of τ is the decisive factor for a defect in the IDC. The equivalent circuit of the lab test setup given in Fig. 8 was evaluated with different values for U_{CS0}. The result is shown in Fig. 11. There is a distinct decrease of τ for U_{CS0} > 16 kV.

The lab measurements shown in Fig. 9 were realized with U_{CS0} = 22 kV (indicated as blue dot in Fig. 11).

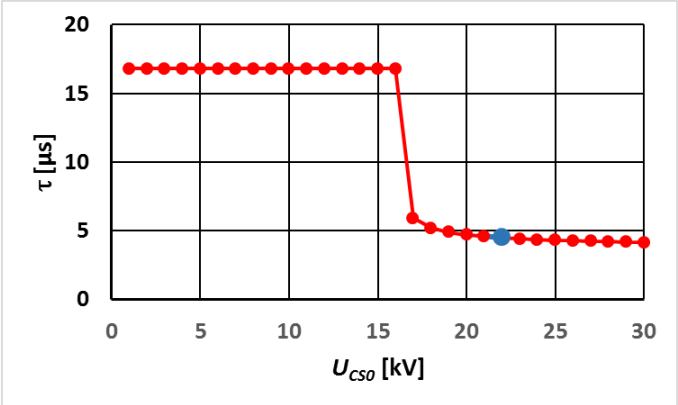

Figure 11. Influence of charging voltage U_{CS0} on time constant τ.

IV. On-site Test Using the Integral Method

This integral detection method was applied in an on-site test at a complex IDC system installed at a factory building. This IDC system consists of 4 branches of IDCs as shown in Fig. 12.

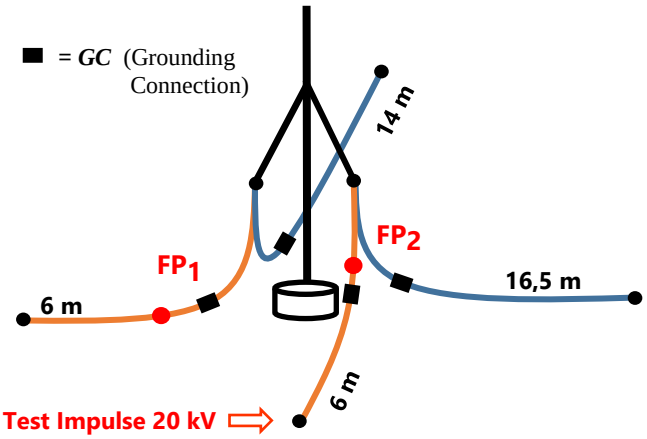

Figure 12. IDC system used for on-site test

Each of these branches has got an individual grounding connection GC located 1,2 m away from the head piece. Two fault positions FP_1 and FP_2 were selected in order to incorporate artificial defects. Only one of the defects was active at one time. FP1 (FP2) is located 1,5 m (0,2 m) away from the next GC.

Three tests were performed. The first test was performed without any defect, the second test with an artificial defect at FP_1 and the third test with an artificial defect at FP_2. The results of these three tests are given in Fig. 13. The upper plots show the time dependence of $u_{CS}(t)$ during the tests (blue trace = without any defect; red trace = defect at FP_1; green trace = defect at FP_2). The three lower plots show the corresponding integrals of $u_{CS}(t)$. The change in the integral of $u_{CS}(t)$ reflects the different time constants (τ).

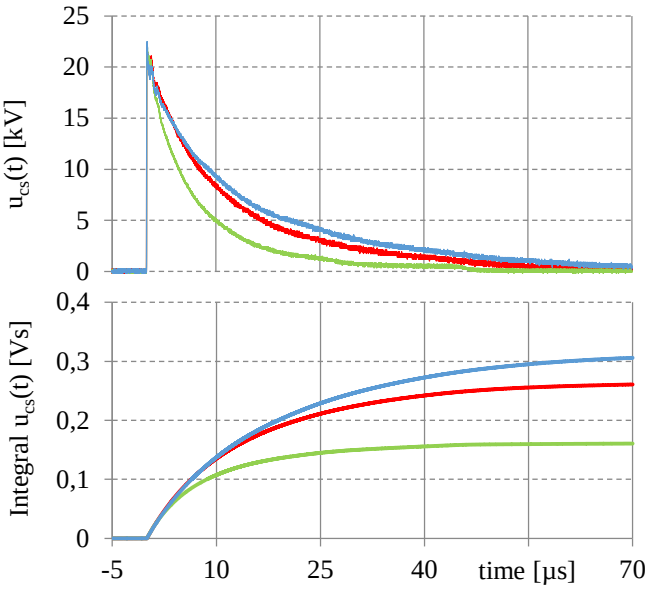

Figure 13. Results of the on-site measurements at the IDC system
blue trace: without any defect
red trace: with artificial defect at FP1
green trace: with artificial defect at FP2

A fault position closer to the next GC (at these tests FP_2 is closer as FP_1) results in a smaller R_F and also in a smaller τ. This is noticeable in Fig. 13 as the green trace is significant below the red trace. If the failure is displaced from the GC the detection becomes more difficult due to the resulting smaller resistive change. In this case both artificial fault positions are well detectable by the integral method. The detection efficiency of failures far apart of the GC (e. g. closer to the injection point) depends on the grounding of the sheath of the IDC. If it is grounded the results come clearer. However this kind of failure is very unlikely because of minimum voltage stress at real lightning in this section. Therefore a dependable failure detection in the region of the GC is of major interest.

V. Conclusions

IDCs may be damaged by mechanical or dielectric overloads or by mistakes done during installation. Not all damage is hard to be detected by inspection during or after installation. Especially a loss of insulation capability is hard to be detected.

The paper presents and discusses new electric test methods for the detection of insulation faults in insulating down conductors (IDCs). Due to the different electromagnetic behavior these test methods differ from those methods which are well known from the diagnostic of power and high frequency cables.

At the present state of knowledge it is necessary to stimulate the defect in such a way that a small discharge occurs at the fault position. A high voltage test impulse with an amplitude in the range of 20…30 kV is injected in the IDC to achieve such a discharge. The nonlinear effects caused by the discharge are detectable and can be used for the fault detection.

These effects have been investigated by comprehensive lab tests on IDCs. A simple but well applicable model of the IDC and the fault behavior is presented and verified by the lab experiments. An implementation of this model in the SPICE program is given and tested.

Different methods for the fault detection based on the transient analysis of the injected high voltage pulse and of the electromagnetic field generated by the discharge at the fault position are discussed by means of the lab experiments. All are applicable for the fault detection in IDCs.

For on-site testing the simple and robust integral method was developed which is to a high degree resistant to interferences. The theoretical background of this method is given as well.

Finally this method was applied for a first on-site test at a real and complex IDC system installed at a factory building. The results of these on-site tests are presented and discussed. The applicability of the integral test method was proved. The future work concentrates on the optimization of the test impulse injection method (surge voltage vs. surge current). Final aim is the minimization of the test impulse energy taking into account the aspects of EMC and safety at on-site testing. The latest work on this topic shows that an inductive loaded hybrid generator circuit minimizes the strain for electronic equipment and persons at the test site.

There is no significant hazard for a person even under worst case conditions. That means the person is touching the grounding connections (GC) of the IDC during the on-site test and an insolation fault occurs at the GC. In this case the pulse energy the person is exposed is below 300 mJ. This is well in the limits for energy (< 350 mJ) of high voltage pulses (>15 kV) given in IEC 61010-1 [7] and there is no hazard of electrical shock. The need for standardization of such tests is also discussed in IEC TC81 WG11.

Acknowledgment

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